AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application. Claims 1-13 are herein amended and claims 14-20 are added.

Listing of Claims

1. (Currently Amended): In a processor having multiple hardware streams supporting multiple data threads, and a data cache, a system for fetching instructions from ~~individual ones~~a selected one of the multiple hardware streams to a pipeline, the system comprising:

multiple hit/miss predictors, each associated with a corresponding one of the multiple hardware streams, said each configured to forecast whether corresponding instructions from said corresponding one of the multiple hardware streams will hit or miss the data cache; and

a fetch algorithm, coupled to said multiple hit/miss predictors, configured to select, on a cycle-by-cycle basis, the selected one of the multiple hardware streams ~~for selecting~~ from which ~~stream~~ to fetch the instructions.~~; and~~

~~a hit/miss predictor for forecasting whether instructions will hit or miss the data cache;~~

~~wherein the prediction by the hit/miss predictor is used by the fetch algorithm in determining from which stream to fetch.~~

2. (Currently Amended): The system as recited in~~of claim 1~~ claim 1, wherein a hit prediction precipitates no change in the fetching of the instructions~~process~~.

3. (Currently Amended): The system as recited in ~~of claim 1~~claim 1, wherein a miss prediction results in switching the fetching~~fetching~~ to a different one of the multiple hardware ~~stream~~streams.

4. (Currently Amended): The system ~~of claim 1~~as recited in claim 1, wherein ~~the hit/miss predictor~~ said each of said multiple hit/miss predictors ~~determines a hit probability~~generates a confidence level value, and ~~the probability is~~ said confidence level value is used by ~~the fetch~~ said fetch algorithm ~~in determining from where to fetch next instructions~~ to select the selected one of the multiple hardware streams.

5. (Currently Amended): The system ~~of claim 1~~ as recited in claim 1, wherein ~~the forecast of the hit/miss predictor is also used by a dispatch algorithm in selecting instructions from the pipeline to dispatch to functional units~~said multiple hit/miss predictors operate at a dispatch level to optimize the dispatch of consumer instructions by predicting latency of data.

6. (Currently Amended): A processor having multiple hardware steams supporting multiple data threads, the processor comprising:

a data cache, comprising a plurality of levels;

multiple hit/miss predictors, each associated with a corresponding one of the multiple hardware streams, said each configured to forecast whether corresponding instructions from said corresponding one of the multiple hardware streams will hit or miss said data cache, said each of said multiple hit/miss predictors comprising:

a plurality of hit/miss predictors, each configured to forecast whether said corresponding instructions from said corresponding one of the multiple hardware streams will hit or miss one or more of said levels; and

a fetch algorithm, coupled to said multiple hit/miss predictors, configured to select, on a cycle-by-cycle basis, the selected one of the multiple hardware streams from which to fetch the instructions, wherein said fetch algorithm selects the selected one of the multiple hardware streams based upon whether said corresponding instructions from said corresponding one of the multiple hardware streams will hit or miss said one or more of said levels.

~~.a fetch algorithm for selecting from which stream to fetch instructions; and~~

~~a hit/miss predictor for predicting whether instructions will hit or miss the cache;~~

~~wherein a prediction by the hit/miss predictor is used by the fetch algorithm in determining from which stream to fetch.~~

7. (Currently Amended): The processor ~~of claim 6~~as recited in claim 6, wherein a hit prediction precipitates no change in the fetching ~~process~~of the instructions.

8. (Currently Amended): The processor as recited in claim 6, ~~of claim 6~~ wherein a miss prediction results in switching the fetching to a different one of the multiple hardware streams~~fetching to a different stream~~.

9. (Currently Amended): The processor ~~of claim 6~~as recited in claim 6, wherein said each of said multiple hit/miss predictors generates a confidence level value, and said confidence level value is used by said fetch algorithm to select the selected one of the multiple hardware streams.~~the hit/miss predictor determines a hit probability, and the probability is used by the fetch algorithm in determining from where to fetch next instructions.~~

10. (Currently Amended): The processor ~~of claim 6~~as recited in claim 6, wherein said multiple hit/miss predictors operate at a dispatch level to optimize the dispatch of consumer instructions by predicting latency of data.~~the forecast of the hit/miss predictor is also used by a dispatch algorithm in selecting instructions from the pipeline to dispatch to functional units.~~

11. (Currently Amended): In a processor having multiple hardware streams supporting multiple ~~data thread,~~data threads, and a data cache, a method for fetching instructions from ~~individual ones~~a selected one of the multiple hardware streams ~~of multiple streams as instruction sources~~ to a pipeline, the method comprising: ~~the steps of:~~

~~(a)~~ for each of the multiple hardware streams, making a hit/miss prediction by ~~a predictor~~ a corresponding one of associated hit/miss predictors as to whether corresponding instructions for the each of the multiple hardware stream previously fetched will hit or miss the data cache; and

~~(b) if the prediction is a miss,~~selecting, on a cycle-by-cycle basis, the selected one of the multiple hardware streams from which to fetch the instructions. ~~altering the source of the fetch.~~

12. (Currently Amended): The method ~~of claim 11~~ as recited in claim 11, wherein ~~the hit/miss predictor determines a hit probability, and the probability is used in determining fetch source~~said making comprises:

generating a confidence level value, and employing the confidence level to select the selected one of the multiple hardware streams.

13. (Currently Amended): The method ~~of claim 11~~as recited in claim 11, ~~wherein the forecast of the hit/miss predictor is also used by a dispatch algorithm in selecting instructions to dispatch to functional units~~further comprising:

operating the multiple hit/miss predictors at a dispatch level to optimize the dispatch of consumer instructions by predicting latency of data.

14. (New): The system as recited in claim 1, wherein the processor comprises a fine-grained multistreaming processor that concurrently executes the instructions from the multiple hardware streams.

15. (New): The system as recited in claim 1, wherein the data cache comprises:

a first level and a second level, and wherein said each of said multiple hit/miss predictors comprises:

a first hit/miss predictor, configured to forecast whether said corresponding instructions from said corresponding one of the multiple hardware streams will hit or miss said first level; and

a second hit/miss predictor, configured to forecast whether said corresponding instructions from said corresponding one of the multiple hardware streams will hit or miss said second level;

wherein said fetch algorithm selects the selected one of the multiple hardware streams based upon whether said corresponding instructions from said corresponding one of the multiple hardware streams will hit or miss said second level.

16. (New): The system as recited in claim 1, wherein the processor comprises a network processor, and wherein said each of said multiple hit/miss predictors employs a flow number to which a packet belongs to forecast whether said corresponding instructions from said corresponding one of the multiple hardware streams will hit or miss the data cache.

17. (New): The processor as recited in claim 6, wherein the processor comprises a network processor, and wherein said each of said multiple hit/miss predictors employs a flow number to which a packet belongs to forecast whether said corresponding instructions from said corresponding one of the multiple hardware streams will hit or miss the data cache.

18. (New): The method as recited in claim 11, wherein said selecting comprises:

switching the fetching to a different one of the multiple hardware streams.

19. (New): The method as recited in claim 11, wherein the data cache comprises a first level and a second level, and wherein said making comprises:

first forecasting whether said corresponding instructions from the corresponding one of the multiple hardware streams will hit or miss the first level; and

second forecasting whether the corresponding instructions from the corresponding one of the multiple hardware streams will hit or miss the second level; and

wherein said selecting comprises:

choosing the selected one of the multiple hardware streams based upon whether the corresponding instructions from the corresponding one of the multiple hardware streams will hit or miss the second level.

20. (New): The method as recited in claim 11, wherein said making comprises:

employing a flow number to which a packet belongs to forecast whether the corresponding instructions from the corresponding one of the multiple hardware streams will hit or miss the data cache.